SOLAR DEVICE STUDIO / PUBLIC EVIDENCE

A 75 um silicon HBC design projection

A source-traceable, target-blind device intervention that clears a 5% modeled relative-gain gate. Fabrication and external validation remain pending.

26.74%	28.513%	+1.390	+5.125%
CERTIFIED PUBLISHED REFERENCE	MODELED 75 um CANDIDATE	PCE POINTS VS MODELED BASELINE	RELATIVE MODELED GAIN

The result in one paragraph

Solar Device Studio used a published 2024 large-area silicon heterojunction back-contact device and its published improvement roadmap. The added intervention is a 75 um wafer, selected by rounding an independent certified 74 um thin-wafer precedent to a 5 um pilot grid before terminal efficiency was calculated. The thinner design is projected at 28.513% PCE. Across the source's 1.2-1.5 ohm-cm resistivity interval, modeled relative gain remains 5.048-5.193%.

Why the proposal is testable

- One process-addressable variable is added: wafer thickness changes from 175 um to 75 um.
- The source roadmap stack is held fixed, including its optical, contact, passivation, edge, and rear-pattern assumptions.
- The thinner device is charged for its predicted optical-current loss before terminal scoring.
- The 5% relative-gain gate passes at the resistivity midpoint and both reported endpoints.

RESEARCH PROJECTION - NOT A MEASURED OR CERTIFIED CELL

Evidence chain

The sequence below separates published evidence, design choice, modeled output, and the missing experiment.

Stage	Evidence or action	Status
Published device	274.3 cm2 certified full-area HBC cell; 175 um wafer; 26.74% PCE.	Measured
Published roadmap	Improved optics, contacts, passivation, edge control, and rear pattern; reported pathway to 27.7%.	Source scenario
Thickness choice	Independent 74 um certified thin-wafer precedent rounded to a 75 um pilot grid before scoring.	Target-blind
Modeled candidate	42.652 mA/cm2 Jsc, 0.7873 V Voc, 0.8492 fill factor, and 28.513% PCE.	Research projection
Decisive next test	Matched three-arm HBC split-lot: 175 um baseline, 175 um roadmap, and 75 um roadmap candidate.	Pending

Known baseline discrepancy

The 175 um baseline replay is 27.123% PCE, 0.383 percentage points above the certified 26.74% result. Absolute replay errors are 0.02745 V in Voc and 0.01886 in fill factor. Published Jsc is an explicit baseline scenario input, so its near-zero replay error is not independent optical validation. HBC therefore remains outside the currently qualified Al-BSF architecture scope.

Hard claim boundary

- Not fabricated, not certified, and not a world-record claim.
- No manufacturing-yield, mechanical-survival, or cost claim is made.
- The optical calculation is a bulk double-pass screen, not a full textured-device ray trace.
- The 74 um precedent is an SHJ cell, not an HBC production demonstration.
- The published roadmap improvements must transfer together to the thin wafer.

Primary sources

Device article: https://doi.org/10.1038/s41467-024-53275-5

Official source data: https://doi.org/10.6084/m9.figshare.26011138

Thin-wafer precedent: https://doi.org/10.1038/s41586-023-06948-y

See sources.md and public-receipt.json for machine-readable provenance.

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